# Aflevering 2

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## Prerequisites

Throughout my assignment I will be setting the body terminal to ground if I’m not asked to do it otherwise.

## Opgave 1

Et billede, der indeholder diagram, skitse, Teknisk tegning, Font/skrifttype

Automatisk genereret beskrivelseIn the following circuit assume that all transistors are operating in the saturation region. Also,

assume that

### Find such that the bias current of M1 is I1 = 1mA

So

As the bias current running through should be , then the voltage at the source should be.

*Ligningen løses for V\_s vha. WordMat.*

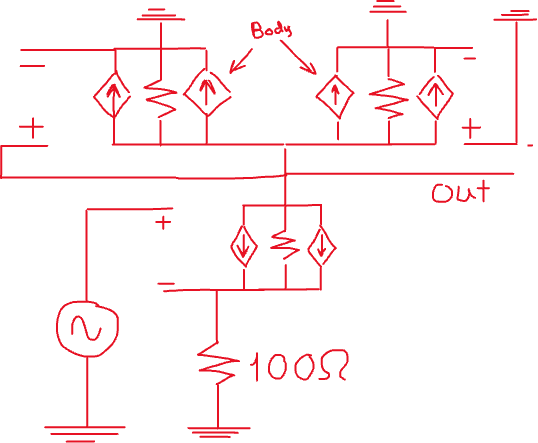
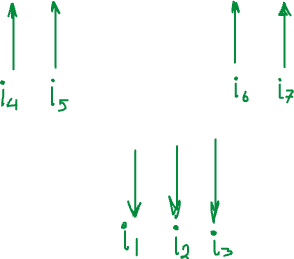
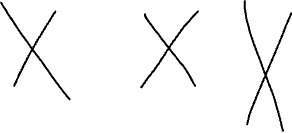
As the source voltage is then 0,1V, then I have

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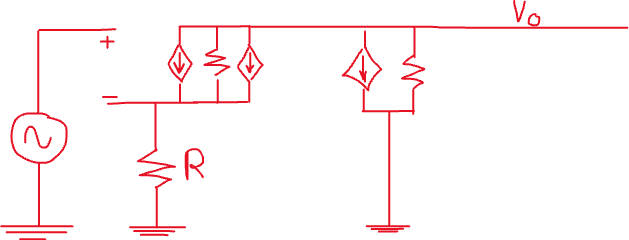
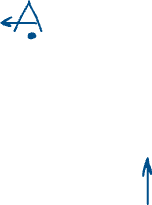
Et billede, der indeholder diagram, skitse, Teknisk tegning, Font/skrifttype

Automatisk genereret beskrivelse

### Calculate the small signal voltage gain



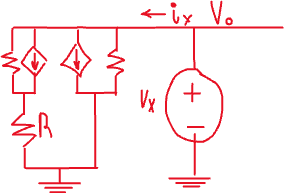
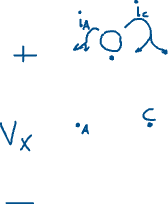
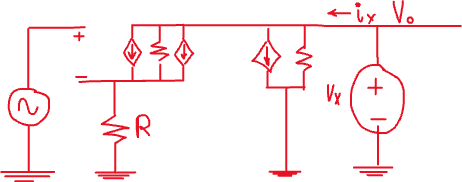
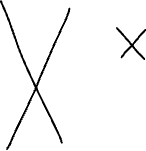
The current entering is the same as the current leaving.



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### Calculate the small signal output impedance seen at the output node

I’ll be sending in a test current ix from my test voltage vx. My other source = 0.



And again, the drain source voltage is only   
depended on the internal resistance.

And let me now describe the second current I described, .

As in saturation, and that we assume that for all.

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So for the minimum Vds VGS == Vth.

Means

## Opgave 2. Common source amplifier with diode connected load

Design a common-source amplifier with a diode-connected load based on the schematic shown below with the following design specifications:

* Transistor M1 is in saturation
* The minimum possible output voltage to keep M1 in saturation is 0.2V
* Et billede, der indeholder diagram, linje/række, skitse, Font/skrifttype

  Automatisk genereret beskrivelseTotal power consumption of the amplifier is 3mW
* Both transistors have L=0.5μm and for transistor M2 we have W2=1 μm

The technology parameters are: λ(NMOS) = 0, ϒ = 0, VDD=3V, VTN = 0.5V, μnCox=1 mA/V2

### Find the following values:

1. DC level of the input
2. DC level of the output
3. Width of transistor M1
4. Small signal gain
5. Maximum output signal swing for a symmetric output signal

So let me check out the specifications first.

#### Specifications

M1 to be in saturation:

Total power consumption of “the” amplifier, so M1?   
Seems so:   
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### Values:

And as should be atleast 0,2V.   
Rearranging  
So according the biasing of Vin should be chosen from:

The height of the small signal sets the criteria for what the biasing term should be.   
I might derive some more information later, but for now:   
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Holds

Et billede, der indeholder Font/skrifttype, håndskrift, tekst, linje/række

Automatisk genereret beskrivelse

Let me look at currents through the transistors.

Så det samme for input transistoren.

Let’s check for the minimum case.   
The output voltage is said to always be bigger than 0,2V. Worst case is when Vout is 0,2V  
Which means, that the biasing term should make sure, that that’s true, atleast.   
No current without ways to drift:

We are just looking at biasing terms right now ( Large signal )

Keeping in mind that

And

And the minimum output would have to be 0,2V.

For the same bias current to run though, it helps that Vin is as large as it can be.

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This means that even with the largest set input voltage, the width of the transistor should be atleast 339,5 times larger.

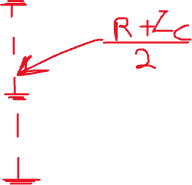
## Opgave 3. Half circuit

In the following circuit assume transistors M1 and M2, and transistors M3 and M4

are identical and ϒ = 0: and λ ≠ 0:

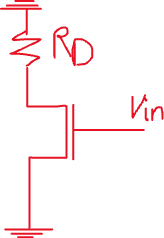
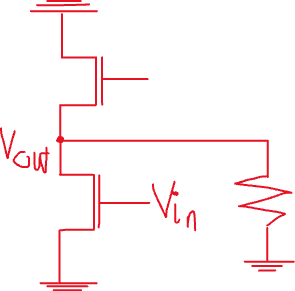
Et billede, der indeholder diagram, linje/række, Plan, Font/skrifttype

Automatisk genereret beskrivelse



I will be viewing the circuit as two symmetric half circuits. By doing that, I can view the center as a virtual ground, and analyze just once side for the gain.

I see, that Vin just experiences an RD and a RS of zero.  
 So this circuit can be viewed as a common source with source  
 degeneration.



And then I find the gain as   
Et billede, der indeholder tekst, fjeder, spiralfjeder, typografi

Automatisk genereret beskrivelse  
And as , , then I will just call the input parts , and bias parts all the transistors are equal.   
   
With

1. Gain for low frequencies:

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If then  
   
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1. Gain for high frequencies:

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If then   
   
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## Opgave 4

Et billede, der indeholder diagram, Font/skrifttype, tekst, linje/række

Automatisk genereret beskrivelseA CMOS amplifier is shown below. Assume M1 and M2 operate in saturation. Values to use:

*Things to note before starting:*I am neglecting the channel length modulation, as these transistors that I’m working with is of large sizes compared to what I could have worked with, say 80nm or even smaller technologies.   
The channel length comes into play, when the technology lengths get to a point, where a change in depletion region causes a non neglectable change in the effective length. And this is by far the smallest of transistors, that I could be working with.

### What value of gives 100 μA through M1 and M2

*Ligningen løses for V\_GG vha. WordMat.*

As

I choose   
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### Et billede, der indeholder tekst, Font/skrifttype, skærmbillede, linje/række Automatisk genereret beskrivelseEt billede, der indeholder Font/skrifttype, tekst, linje/række, skærmbillede Automatisk genereret beskrivelseEt billede, der indeholder diagram, Font/skrifttype, tekst, linje/række Automatisk genereret beskrivelseWhat’s the dc value of Vin



Inserting eq. 3 into eq. 2

Now substituting  
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Et billede, der indeholder diagram, Font/skrifttype, tekst, linje/række

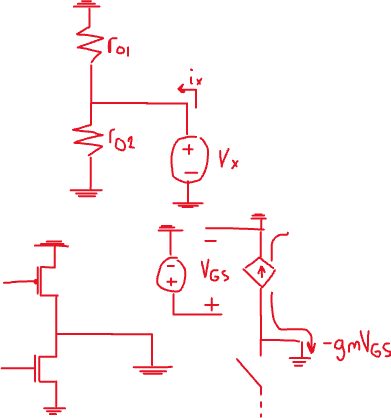
Automatisk genereret beskrivelse

### What’s the small signal gain for this circuit.

The gain can be written as   
So let me solve the circuit for these values.   
*Rout*



*Gm*



So far so good, but I know that   
   
Has the wrong sign for this circuit. It’s supposed to be negative, due to the pmos being the input.   
When solving for output resistance, I solved for a current coming from output. For the transconductance, I solved for a current to the output.  
The sign seems wrong, but I think I might just have the right gain.   
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## Et billede, der indeholder diagram, tekst, Teknisk tegning, Plan Automatisk genereret beskrivelseOpgave 5. Characterize the circuits.

I need to solve for 2 circuits.

I will be calculating in the sector underneath, and only give guided solutions here, followed by the answer.   
   
Answers:

### *Circuit*

Using half circuit technique I see a cascode pmos network Cp, and a cascode nmos network Cn, where the bottom nmos is the input.

So

When shorting the output to find the transconductance, only the nmos network is used in the circuit. Pmos network is open.

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**Output swing**I’ve already solved for the gain.   
   
   
   
   
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**Vin, cm range**

At minimum, the input transistors should be at saturation.

### Circuit.

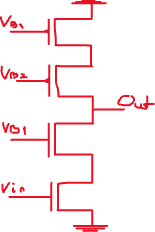
**Gain**

Solved current for every path to find the output resistance to be.

## Et billede, der indeholder diagram, Font/skrifttype, linje/række, tekst Automatisk genereret beskrivelseOpgave 5. Theory behind answers:

These circuits looks doable with half circuit techniques.

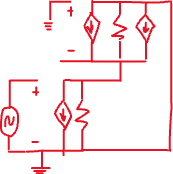
*Circuit a*   
**Gain**  
For finding the Rout I could   
Solve for the different behaviors due to cascade.   
But I have a formula, which has it solved:



Et billede, der indeholder diagram, Font/skrifttype, linje/række, design

Automatisk genereret beskrivelseAnd I have transistors in cascade in the pmos   
network, and in the nmos network.

  
Solving for the transconductance:

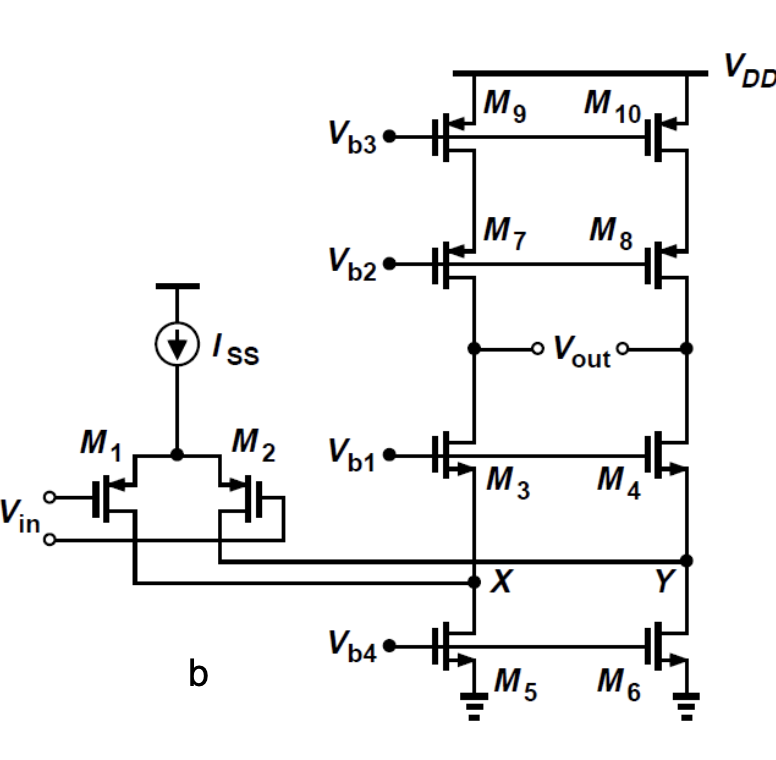


Inserting eq. 1 into eq. 2   
The impedance is found from the current running to output divided by the gate source voltage. In this case:

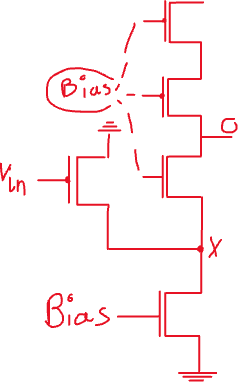
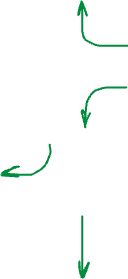
But we want it to be due to Vin

Inserting this back into equation 1.

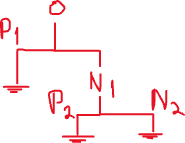
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**Circuit b.**

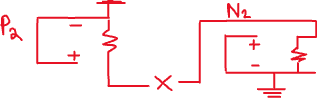
**Gain**



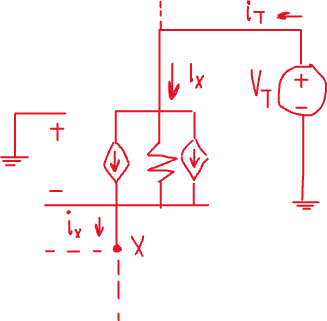
Finding the output resistance.   
 The output sees a pmos network and a “Nmos” network From the nmos network, it then travels through a  
 transistor, sees a pmos network, and a nmos network.



So let me just get the resistances of these paths.

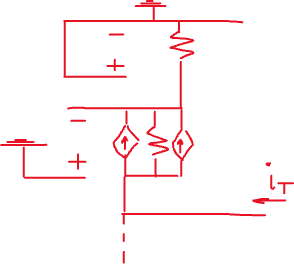


So the parallel connection only has   
internal resistance to affect the system.   
   
   
  
Looking at M3:



Inserting eq. 1 into eq. 2.

For the pmos network



Inserting eq. 5 into eq. 4



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## Ekstra

### Tried to solve for numeric value of gain to circuit a.

Assuming that the pmos is set in size to compensate for the lag of mobility. This set to be a factor of two, then:

Et billede, der indeholder tekst, Font/skrifttype, skærmbillede, nummer/tal

Automatisk genereret beskrivelse



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### Output swing calculations

Et billede, der indeholder diagram, Font/skrifttype, linje/række, tekst

Automatisk genereret beskrivelseThe swing is the amplitude. The difference in voltages / 2 at the time of maximum should then equal the swing.   
When looking at this circuit, it reaches it swing when  
   
   
The Y is phaseshifted by 180° as I see it, having - Vin at it’s gate.   
For this to work, the bias transistors should be in saturation, ideally at overdrive voltage.



Neglecting the body effect

For our course our effective channel length modulation is at for nmos and for pmos.   
As the bias voltages have been set to overdrive voltage, that can be found by:

Recognizing that the current through X side + the current through the Y side I have:

Suggesting that

### More output swing calculations attempt

Et billede, der indeholder diagram, Font/skrifttype, linje/række

Automatisk genereret beskrivelseFor the biggest swing, the bias voltages should only be sufficient for saturation region.   
, then   
And takes it maximum values, when the source gate voltages are just sufficient, for saturation. *When the source gates voltages are at their minimum.*

If I look at my pmos network in terms of an equivalent resistance, then I can with the knowing of currents running through the network, derive what the maximum voltage could be.

I did this at the gain section.   
   
Then the maximum should be:   
As the inputs’ are of equal magnitudes

